



M.A.M. SCHOOL OF ENGINEERING

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Siruganur, Trichy -621 105.

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2.5.1 Mechanism of internal assessment is transparent and robust in terms of frequency and variety

The college examination cell conducts Continuous Internal Assessment (CIA) and University Examinations as per the guidelines of the University. In order to ensure transparency in CIA is given in Academic calendar which is displayed well in advance before commencement of session. The subject handling faculty prepares question bank with PART-A and PART-B to the students in advance for CIA -I and CIA -II and MODEL exam. The question papers are verified by the subject experts and HOD to strengthen the quality of question paper. To avoid the malpractice and observation, squad teams are assigned from our institution to monitor the internal assessment. The evaluated answer papers are distributed to the students within two days after the exam and the answers are discussed. Special coaching classes are conducted for students who fail to secure the minimum percentage of marks. Retests are conducted for the failed students after the working hours. All the test marks are entered into the university web portal as scheduled by the assessment period and it will also be viewed by the students using their login id and password. All the CIA marks are displayed in the department notice board and are informed to parents through postal communication. The institution continuously reviews the evaluation process done internally and necessary changes as and when required are implemented. There are three tests which form part of internal evaluation for every subject. The institute encourages the faculty to experiment with various evaluation techniques to test learning of students. For assessment of project, faculty coordinator prepares a schedule of presentation of students in slots in consultation with the HOD and Principal and is communicated to students. Students present their work or report to the coordinator via PPT mode and evaluated on the basis of various parameter set by respective coordinator. For assessment of laboratory course an internal practical viva conducted by respective faculty member at the end of course. In addition to the above, regular assignments and seminar presentation are also part of the evaluation process. In this way mechanism of internal assessment is transparent and robust.

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2.5.1 Mechanism of internal assessment is transparent and robust in terms of frequency and variety

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M.A.M. SCHOOL OF ENGINEERING (Accredited by NAAC) Trichy -621 105				
Academic Calendar 2019-20 (Even Semester) Dec 2019 - April 2020				
Date and Day	Description	Activity Count	Working Day	Activity
Monday, December 16, 2019	Reopening Day For IV, VI & VIII SEMESTERS	1	1	
Tuesday, December 17, 2019		2	2	
Wednesday, December 18, 2019		3	3	
Thursday, December 19, 2019		4	4	
Friday, December 20, 2019		5	5	
Saturday, December 21, 2019				
Sunday, December 22, 2019	Holiday			
Monday, December 23, 2019	Holiday			
Tuesday, December 24, 2019	Holiday			
Wednesday, December 25, 2019	Holiday - Christmas			
Thursday, December 26, 2019	Holiday			
Friday, December 27, 2019	Holiday			
Saturday, December 28, 2019	Holiday			
Sunday, December 29, 2019	Holiday			
Monday, December 30, 2019	Holiday			
Tuesday, December 31, 2019	Holiday			
Wednesday, January 01, 2020	Holiday - New Year			
Thursday, January 02, 2020		6	6	
Friday, January 03, 2020	Unit 1.5 Portion Completion	7	7	
Saturday, January 04, 2020	Holiday - First Saturday			
Sunday, January 05, 2020	Holiday			
Monday, January 06, 2020		8	8	First Class Committee Meeting-Final Year
Tuesday, January 07, 2020	U I-Sub1	9	9	First Class Committee Meeting-Third Year
Wednesday, January 08, 2020	U I-Sub12	10	10	First Class Committee Meeting-Second Year
Thursday, January 09, 2020	U I-Sub3	11	11	First Online Feed Back-Final Year
Friday, January 10, 2020	U I-Sub4	12	12	First Online Feed Back-Third Year
Saturday, January 11, 2020	U I-Sub5	13	13	First Online Feed Back-Second Year
Sunday, January 12, 2020	Holiday			
Monday, January 13, 2020	U I-Sub6	14	14	
Tuesday, January 14, 2020	Holiday			
Wednesday, January 15, 2020	Holiday - Pongal			
Thursday, January 16, 2020	Holiday - Thiruvalluvar Day			
Friday, January 17, 2020	Holiday - Ulaavar Thirunal			
Saturday, January 18, 2020	Holiday			
Sunday, January 19, 2020	Holiday			
Monday, January 20, 2020		15	15	
Tuesday, January 21, 2020		16	16	
Wednesday, January 22, 2020		17	17	
Thursday, January 23, 2020		18	18	
Friday, January 24, 2020		19	19	
Saturday, January 25, 2020	Unit 2 Portion Completion	20	20	
Sunday, January 26, 2020	Holiday - Republic Day			
Monday, January 27, 2020	CIA I-Sub1		21	
Tuesday, January 28, 2020	CIA I-Sub2		22	
Wednesday, January 29, 2020	CIA I-Sub3		23	
Thursday, January 30, 2020	CIA I-Sub4		24	
Friday, January 31, 2020	CIA I-Sub5		25	
Saturday, February 01, 2020	CIA I-Sub6		26	
Sunday, February 02, 2020	Holiday			
Monday, February 03, 2020	Unit 3 Starts	1	27	
Tuesday, February 04, 2020		2	28	
Wednesday, February 05, 2020		3	29	
Thursday, February 06, 2020		4	30	
Friday, February 07, 2020		5	31	
Saturday, February 08, 2020		6	32	
Sunday, February 09, 2020	Holiday			
Monday, February 10, 2020		7	33	
Tuesday, February 11, 2020	UNIT 3 PORTION COMPLETION	8	34	Second Class Committee Meeting-Final Year
Wednesday, February 12, 2020		9	35	Second Class Committee Meeting-Third Year
Thursday, February 13, 2020		10	36	Second Class Committee Meeting-Second Year
Friday, February 14, 2020		11	37	
Saturday, February 15, 2020		12	38	
Sunday, February 16, 2020	Holiday			



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Academic Calendar

Monday, February 17, 2020		13	59	Second Order Feed Back Final Year
Tuesday, February 18, 2020		14	40	Second Order Feed Back Third Year
Wednesday, February 19, 2020		15	41	Second Order Feed Back Second Year
Thursday, February 20, 2020	UNIT 4 FORMATION COMPLETION	16	42	
Friday, February 21, 2020	COACHING LAB 1		43	
Saturday, February 22, 2020	Holiday			
Sunday, February 23, 2020				
Monday, February 24, 2020	CIA II-Sub1		44	
Tuesday, February 25, 2020	CIA II-Sub2		45	
Wednesday, February 26, 2020	CIA II-Sub3		46	
Thursday, February 27, 2020	CIA II-Sub4		47	
Friday, February 28, 2020	CIA II-Sub5		48	
Saturday, February 29, 2020	CIA II-Sub6		49	
Sunday, March 01, 2020	Holiday			
Monday, March 02, 2020		1	50	
Tuesday, March 03, 2020		2	51	
Wednesday, March 04, 2020		3	52	
Thursday, March 05, 2020		4	53	
Friday, March 06, 2020	UNIT 5 Process Control	5	54	Process Data & SIMPLIFIED
Saturday, March 07, 2020	CIA III-Sub1		55	
Sunday, March 08, 2020	Holiday			
Monday, March 09, 2020	CIA III-Sub2		56	
Tuesday, March 10, 2020	CIA III-Sub3		57	Third Class Committee Meeting Final Year
Wednesday, March 11, 2020	CIA III-Sub4		58	Third Class Committee Meeting Third Year
Thursday, March 12, 2020	CIA III-Sub5		59	Third Class Committee Meeting Second Year
Friday, March 13, 2020	CIA III-Sub6		60	
Saturday, March 14, 2020			61	
Sunday, March 15, 2020	Holiday			
Monday, March 16, 2020			62	
Tuesday, March 17, 2020	Model - Sub 1 AN		63	Third Order Feed Back Final Year
Wednesday, March 18, 2020			64	Third Order Feed Back Third Year
Thursday, March 19, 2020	Model - Sub 2 AN		65	Third Order Feed Back Second Year
Friday, March 20, 2020			66	
Saturday, March 21, 2020	Model - Sub 3 AN		67	
Sunday, March 22, 2020	Holiday			
Monday, March 23, 2020			68	
Tuesday, March 24, 2020	Model - Sub 4 AN		69	
Wednesday, March 25, 2020			70	
Thursday, March 26, 2020	Model - Sub 5 AN		71	
Friday, March 27, 2020			72	
Saturday, March 28, 2020	Model - Sub 6 AN		73	
Sunday, March 29, 2020	Holiday			
Monday, March 30, 2020	Model Retest - Sub 1 AN Model Practical		74	
Tuesday, March 31, 2020	Model Retest - Sub 2 AN Model Practical		75	
Wednesday, April 01, 2020	Model Retest - Sub 3 AN Model Practical		76	
Thursday, April 02, 2020	Model Retest - Sub 4 AN		77	
Friday, April 03, 2020	Model Retest - Sub 5 AN		78	
Saturday, April 04, 2020	Model Retest - Sub 6 AN		79	
Sunday, April 05, 2020	Holiday			
Monday, April 06, 2020				
Tuesday, April 07, 2020				
Wednesday, April 08, 2020				
Thursday, April 09, 2020				
Friday, April 10, 2020	Holiday - Good Friday			
Saturday, April 11, 2020	Holiday			
Sunday, April 12, 2020	Holiday			
Monday, April 13, 2020	Holiday			
Tuesday, April 14, 2020	Holiday - Tamil New Year			
Wednesday, April 15, 2020				
Thursday, April 16, 2020				
Friday, April 17, 2020	IV, VI & VII - Commencement of End Semester Examinations			
Saturday, April 18, 2020				
Sunday, April 19, 2020	Holiday			
Monday, April 20, 2020				
Tuesday, April 21, 2020				
Wednesday, April 22, 2020				
Thursday, April 23, 2020				
Friday, April 24, 2020				
Saturday, April 25, 2020				
Sunday, April 26, 2020	Holiday			
Monday, April 27, 2020				
Tuesday, April 28, 2020				
Wednesday, April 29, 2020				
Thursday, April 30, 2020				

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Exam Cell

Ref: MAMSE/ACD/2019- 20/Even/01	Date: 24.01.2020
Origination: Principal	Classification: Routine
Subject : CIA TEST - I	

The CIA TEST - I examination for II, III & IV B.E students will start from **27.01.2020** and time table is displayed on the notice board. The scheduled time for the test is from **1.30 p.m. to 4.30 p.m.** The portion for the test will be first **TWO UNIT**. All the students are asked to assemble in their respective seats by 1.20 p.m and the students ^{are not} are not permitted into the exam hall after 1.20 p.m. The students are asked to bring all the required test note, question bank and stationery items.

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Dr. P.RANJITH KUMAR, M.E., Ph.D.,
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Circulated to

The HOD, Staff – All departments

All II, III & IV year classes

Notice board

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M.A.M. School of Engineering

ACADEMIC YEAR 2019-2020

CIA TEST-II (Semester: EVEN)



Timing : 1.30 PM TO 4.30 PM				
Dept	Dates	IV-Year	III Year	II Year
AERO	27.01.2020	AE6015-RA3	AE6003 - CMS	AE6404 - Prop-1
	28.01.2020	AE6801-WTT	AE6005 - ESA	AE6401 - AD-I
	29.01.2020		AE6002 - EAD	PR6451 - MM
	30.01.2020		AE6001 - FEM	AE6403 - AS-1
	31.01.2020		GE8075 - IPR	AE6402 - ACS&I
	01.02.2020		AE6004 - AD	MA6491 - NM
CSE	27.01.2020	CS6801-MCA & P	CS6501 - IP	CS6493 - OS
	28.01.2020	CS6008 - HCI	CS6091 - AI	CS6494 - SE
	29.01.2020	MG6088-SPM	CS6001 - MC	CS6451-DAA
	30.01.2020		CS6002 - CD	CS6491-CA
	31.01.2020		GE8075 - IPR	CS6492 - DMS
	01.02.2020		CS6603 - DS	MA6402 - PQT
EEE	27.01.2020	EE6801-EEG&UC	EE6801 - SSD	EE6451-LIC
	28.01.2020	EC6003 - POR	RO8591 - POR	EE6403 - M & I
	29.01.2020	GE6757-TQM	EE6602 - P & SG	EE6402 - T & D
	30.01.2020		EE6091 - ES	EC6451-CS
	31.01.2020		GE8075 - IPR	EE6401-EM-1
	01.02.2020			MA6491 - NM
ECE	27.01.2020	CS6003-ASN	EC6591 - NPMC	MA6451-PRP
	28.01.2020	MG6071-ED	EC6065 - VLSI	EC6452-EC-II
	29.01.2020	EC6801-WC	EC6652 - WC	GE6291-EVS
	30.01.2020	EC6802-WN	EC6591 - POM	EC6451-EMF
	31.01.2020		GE8075 - IPR	EC6491-CT
	01.02.2020		EC6602 - TLR	EC6453 - LIC
MECH	27.01.2020	MG6863-EE	ME6893 - HMT	ME6492-KOM
	28.01.2020	MG6071-ED	ME6891 - CAD&M	ME6453-TE-I
	29.01.2020	ME6016-AICE	ME6694 - HRP	ME6451-MT-II
	30.01.2020		ME6092 - FFA	ME6491-EM
	31.01.2020		GE8075 - IPR	MA6452-SNM
	01.02.2020		ME6851 - DOTS	CE6395-SOM
MECHT	27.01.2020	MT6801-AME	ME6591 - AHP	ME6492-KOM
	28.01.2020	MG6071-ED	MT6801 - DOMS	ME6392-MT
	29.01.2020	MG6088-SPM	ME6593 - DME	MT6491-M&M
	30.01.2020		MG6591 - POM	MT6401-THT
	31.01.2020		GE8075 - IPR	MA6452-SNM
	01.02.2020		MT6602 - IA	

Dr. P. RANJITH KAN, M.Tech, Ph.D.

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HALL NO:AB 304

ROW 1		ROW 2		ROW 3		ROW 4		ROW 5	
IV MECH		IV CSE		IV MECH		IV CSE		IV MECH	
1	812116114001	6	812116104001	11	812116114006	16	812116104008	21	812116114012
2	812116114002	7	812116104003	12	812116114007	17	812116104010	22	812116114013
3	812116114003	8	812116104004	13	812116114008	18	812116104011	23	812116114014
4	812116114004	9	812116104005	14	812116114010	19	812116104012	24	812116114015
5	812116114005	10	812116104007	15	812116114011	20	812116104014	25	812116114016

Principal

M.A.M. SCHOOL OF ENGINEERING, SIRUGANUR, TIRUCHIRAPPALLI CIA-I TEST HALL PLAN

HALL NO:AB 305

ROW 1		ROW 2		ROW 3		ROW 4		ROW 5	
IV MECH		IV CSE		IV MECH		IV CSE / IV ECE		IV MECH	
1	812116114017	6	812116104015	11	812116114023	16	812116104026	21	812116114028
2	812116114018	7	812116104019	12	812116114024	17	812116104027	22	812116114029
3	812116114019	8	812116104020	13	812116114025	18	812116104028	23	812116114030
4	812116114020	9	812116104023	14	812116114026	19	812116105002	24	812116114031
5	812116114021	10	812116104025	15	812116114027	20	812116106003	25	812116114035

Principal

M.A.M. SCHOOL OF ENGINEERING, SIRUGANUR, TIRUCHIRAPPALLI CIA-I TEST HALL PLAN

HALL NO:AB 306

ROW 1		ROW 2		ROW 3		ROW 4		ROW 5	
IV MECH		IV ECE		IV MECH		IV ECE		IV MECH	
1	812116114036	7	812116106004	13	812116114042	19	812116106012	25	812116114048
2	812116114037	8	812116106007	14	812116114043	20	812116106013	26	812116114050
3	812116114038	9	812116106008	15	812116114044	21	812116106014	27	812116114051
4	812116114039	10	812116106009	16	812116114045	22	812116106015	28	812116114052
5	812116114040	11	812116106010	17	812116114046	23	812116106016	29	812116114053
6	812116114041	12	812116106011	18	812116114047	24	812116106017	30	812116114054

Principal

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M.A.M. School of Engineering CIA - 1 Exam Invigilation Duty List

Date: 28.01.2020

S.No	HALL NO.	No. of Students	DEPT	NAME OF THE FACULTY	TIME	SIGNATURE
1	MB205	50	MECH	Mr.G.Karthikeyan	12.53	<i>[Signature]</i>
2			AERO	Dr.K.Chandrasekaran	12.53	<i>[Signature]</i>
3	MB302	50	CSE	V.Vidhya	12.53	<i>[Signature]</i>
4			AERO	Mr.K.M.Sridhar	1.00	<i>[Signature]</i>
5	MB304	50	ECE	Mrs.K.Umarani	1.00	<i>[Signature]</i>
6			MCT	Mrs.P.Sutha	12.50	<i>[Signature]</i>
7	MB305	58	EEE	Ms.Vinothini	1.05	<i>[Signature]</i>
8			EEE	Mr.G.Purusothaman	12.40	<i>[Signature]</i>
9	MB307	50	ECE	G.Sathish Kumar	12.50	<i>[Signature]</i>
10			MECH	M.Manikandan	1.03	<i>[Signature]</i>
11	MB308	49	CSE	G.Rajesh Kumar	12.55	<i>[Signature]</i>
12			MECH	K.Parthiban	1.00	<i>[Signature]</i>
13	AB304	25	MECH	Vimalkumar	1.00	<i>[Signature]</i>
14	AB305	25	CSE	Ms.Murugavalli (Ms.C.Meena)	12.53	<i>[Signature]</i>
15	AB306	30	MCT	S.Saravanan	12.47	<i>[Signature]</i>
16	DH-1	40	AERO	Ms.V.Priyadarsini	12.50	<i>[Signature]</i>
17	DH-2	50	MCT	S.Ravichandran	12.47	<i>[Signature]</i>
18			ECE	K.Karthikeyan A.Karabaskumar	12.47	<i>[Signature]</i>

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Squad Report

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CIA-I EXAMINATIONS

SQUAD REPORT

DATE: 24/1/20

HALL NO: 207

HALL INVIGILATOR NAME: Sri Senthamani Karun

TIME IN:

TIME OUT:

OBSERVATIONS:

* Classroom is not cleaned properly.
Many tiny papers were thrown on the floor.

SIGNATURE OF THE
HALL INVIGILATOR

SQUAD MEMBERS SIGNATURE

- 1) [Signature]
- 2) [Signature]
- 3) [Signature]

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CIA-I EXAMINATIONS

SQUAD REPORT

DATE: 24/1/20

HALL NO: 206

HALL INVIGILATOR NAME: S. Beetha Mang

TIME IN:

TIME OUT:

OBSERVATIONS:

SIGNATURE OF THE
HALL INVIGILATOR

SQUAD MEMBERS SIGNATURE

- 1) [Signature]
- 2) [Signature]
- 3) [Signature]

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ATTENDANCE SHEET FOR CIA EXAM-I

HALL NO: MB-304

Sl.No	Dept	Reg. Number	Name of the Student	27.01.20	28.01.20	29.01.20	30.01.20	31.01.20	01.02.20
1	MECH	81217114054	VIGNY K	AB	AB	AB	AB	AB	AB
2	MECH	81217114088	VIGNAYARATHIN V	AB	AB	AB	AB	AB	AB
3	MECH	81217114089	VIMALUJ K	AB	AB	AB	AB	AB	AB
4	MECH	81217114089	VINITH O P S H P	AB	AB	AB	AB	AB	AB
5	MECH	81217114092	MURALID	AB	AB	AB	AB	AB	AB
6	MECH	81217114301	LOGESH P	AB	AB	AB	AB	AB	AB
7	MECH	81217114303	SYED MUSHTAQ R	AB	AB	AB	AB	AB	AB
8	MECH	81217114701	BALAMURUGAN S	AB	AB	AB	AB	AB	AB
9	MECH	81217114702	SATHYASEELAN C	AB	AB	AB	AB	AB	AB
10	MCT	81217115000	Almond Rishab S	AB	AB	AB	AB	AB	AB
11	MCT	81217115001	A. Bala	AB	AB	AB	AB	AB	AB
12	MCT	81217115004	Indrakrishnan T	AB	AB	AB	AB	AB	AB
13	MCT	81217115005	Id. Deepak	AB	AB	AB	AB	AB	AB
14	MCT	81217115006	Harisharan C	AB	AB	AB	AB	AB	AB
15	MCT	81217115008	Harisharan A	AB	AB	AB	AB	AB	AB
16	MCT	81217115010	Jagadeeswaran K	AB	AB	AB	AB	AB	AB
17	MCT	81217115011	Madhavan N	AB	AB	AB	AB	AB	AB
18	MCT	81217115012	Mohamed Ashik N	AB	AB	AB	AB	AB	AB
19	MCT	81217115013	Mohamed Fahad S	AB	AB	AB	AB	AB	AB
20	MCT	81217115014	Mohamed Faisel M E	AB	AB	AB	AB	AB	AB
21	MCT	81217115015	Mohamed Rishab I	AB	AB	AB	AB	AB	AB
22	MCT	81217115016	M.R.Mohamed Haseeb	AB	AB	AB	AB	AB	AB
23	MCT	81217115017	Mohamed Naveed M	AB	AB	AB	AB	AB	AB
24	MCT	81217115018	Niyas Ahmed S	AB	AB	AB	AB	AB	AB
25	MCT	81217115019	Parthiban R	AB	AB	AB	AB	AB	AB



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Internal Exam Cell

CIA - I - Absentees List

Date of Exam: 28.01.2020/ AN

Sl.No	Year & Dept	Strength	Reg. Number of Absentees	Total No. of Abs
1	II -AERO	24	02,03,07,13,20,21,27,	7
2	II- CSE	24	04,06,08,25,	4
3	II- ECE	14	01,02,14,	3
4	II- EEE	19	01,02,03,10,11,13,18,22,	8
5	II-MECH	34	02,14,16,20,27,	5
7	II-MECHTR	23	06,14,18,26,301,302	6
8	III-AERO	27	06,08,09,31,36,40	6
9	III-CSE	22	17,20,28,	3
10	III-ECE	18	05,08,	2
11	III-EEE	18	28,301,302,	3
12	III-MECH	59	02,07,15,28,36,54,56,64,66,69,70,83, 92,301,701,	15
13	III-MECHTR	26	02,18	2
14	IV- AERO	28	01,06,09,26,501	5
15	IV- CSE	18	10,	1
16	IV- ECE	18	03,	1
17	IV -EEE	20	21,23,25,28	4
18	IV-MECH	68	01,03,04,06,14,16,18,28,35,42,43,47,53,58,69,	15
19	IV-MECHTR	17	04,06,11,18	4
Total strength		477	Total Absentees:	94

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DEPARTMENT OF COMPUTER SCIENCE AND
ENGINEERING

CS8493 - OPERATING SYSTEMS

Question Bank

II YEAR/ BATCH : 2017 -21

UNIT I			
OPERATING SYSTEMS OVERVIEW			
Computer System Overview: Host System, Secondary Storage, Memory, Network, Hardware Configuration, User Interface, Operating System and Network Configuration, Operating System: Overview, Objectives and Functions, Evolution of Operating System, Computer System Organization, Operating System Structure and Operating System Call, System Programs, CPU Scheduling and System Run			
PART A			
S. No.	Question	CO	Bloom Taxonomy Level
1	What are the objectives of operating system? (AO: April/May 2018) (AO: May/June 2012) (April/May 2017)	C01.1	BT-4
2	What are the advantages of peer-to-peer systems over client-server systems? (May/June 2016)	C01.1	BT-4
3	What is the purpose of system programs in an OS? (May/June 2016) (April/May 2018)	C01.1	BT-4

4	What does an interrupt differ from a trap? (Nov/Dec 2016/Apr/May 2018)	C01.1	BT-4
5	What are disadvantages of multiprocessor systems? (Nov/Dec 2016)	C01.1	BT-4
6	Define Round Robin differ from multiprogramming? (Nov/Dec 2016/Apr/May 2018)	C01.1	BT-4
7	Why API's used or favored rather than system call? (April/May 2018)	C01.1	BT-4



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CIATest – 1

CS8493– Operating System

Date: 07-01-2020
Year/Dept:II/CSE

Duration: 1.30pm
Max. Marks:50

Part A (2 Marks)

1. What are the advantages of peer-to-peer systems over client-server systems?
2. What is the purpose of system programs/system calls?
3. How does an interrupt differ from a trap?
4. How does time sharing differ from multiprogramming? If so, how?
5. Compare and contrast DMA and cache memory.
6. Distinguish between batch systems and time sharing systems.
7. Some computer systems do not provide a privileged mode of operation in hardware. Is it possible to construct a secure operating system for these computer systems?
8. Can traps be generated intentionally by a user program? If so, for what purpose?
9. Compare tightly coupled systems and loosely coupled systems?
10. What is dual mode operation and what is the need of it?
11. What is real time system?
12. Discuss the difference between symmetric and asymmetric multiprocessing.
13. Distinguish between hard real time systems and soft real time systems.
14. Define: Clustered systems.
15. What are the three main purposes of an operating system?

Part B (13 Marks)

16. i) Discuss the pros and cons of single processor system, multicore system and clustered system.
ii) Explain the various system calls with example.
17. i) Explain the steps involved to transfer the stored historical information in a magnetic tape to the CPU for further processing through various storage devices.
ii) Explain in detail about DMA.
18. i) Discuss the essential properties of the following types of systems:
a) Time sharing systems b) Multi-processor systems c) Distributed systems
ii) Discuss the functionality of system boot with respect to an operating system.
19. i) Explain in detail about cache memory.
ii) Discuss in detail how the instructions are executed.
20. i) Explain the various services provided by OS.
ii) Explain the various types of system calls with examples.

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8/1/2020

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CS 8493 - Operating
System.

Reg No: 81A118104017

Name: S Preetika

Sub: CS 8493 CS

Date: 11/1/2020

Exam: (IA) Test - 1

Dept: CSE II - Year

Part - A

1) The advantages of peer-to-peer systems
over client-server system.

* The main advantage of peer to peer system over client-server system is that is easier to set up

* The peer to peer system is cost efficient or less expensive

* In peer to peer system, all the nodes are server as well as client, therefore there is no need for dedicated server.

3) Interrupt Differ from a trap

* Interrupt is a hardware generated signal in which the flow of the signal changed within the system. The interrupt CPU does not need CPU hard cycle

* While trap is a software generated interrupt. Trap is mainly used to catch the



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8) Traps

* Traps in a software generating interrupt. The traps be generated unintentionally by a user program, because the traps are mainly used to catch the arithmetic errors.

9) Loosely Coupled Systems

* In loosely coupled system, each processor has its own memory.

* They are communicate with each other through communication wise.

Tightly Coupled System

* In Tightly coupled system, every processor has connected to a single memory.

* They has no communication wise.

11) Real Time System

* A real time system is well defined and has fixed time constraints. The real time system gives guarantee, to process the data in the given constrain.

* The process will be done within the given fixed constrain, otherwise the process will be out.

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Part - B

14) ii)

Direct Memory Access

DMA $\Rightarrow$ Direct Memory Access

* Direct memory access is a method of transferring the data from the computer RAM [Random Access Memory] to the other parts of the computer without processing the data using CPU [Central processing unit].

* Generally many input and output data from the computer is processed by the central processing unit. But some data does not need to process, so such a data are accessed directly by the direct memory access.

* Accessing the data directly, without processing it in CPU is called direct memory access process.

* Direct memory access function will be performed by the direct memory access module which is in the system bus. are incorporated with the I/O devices.

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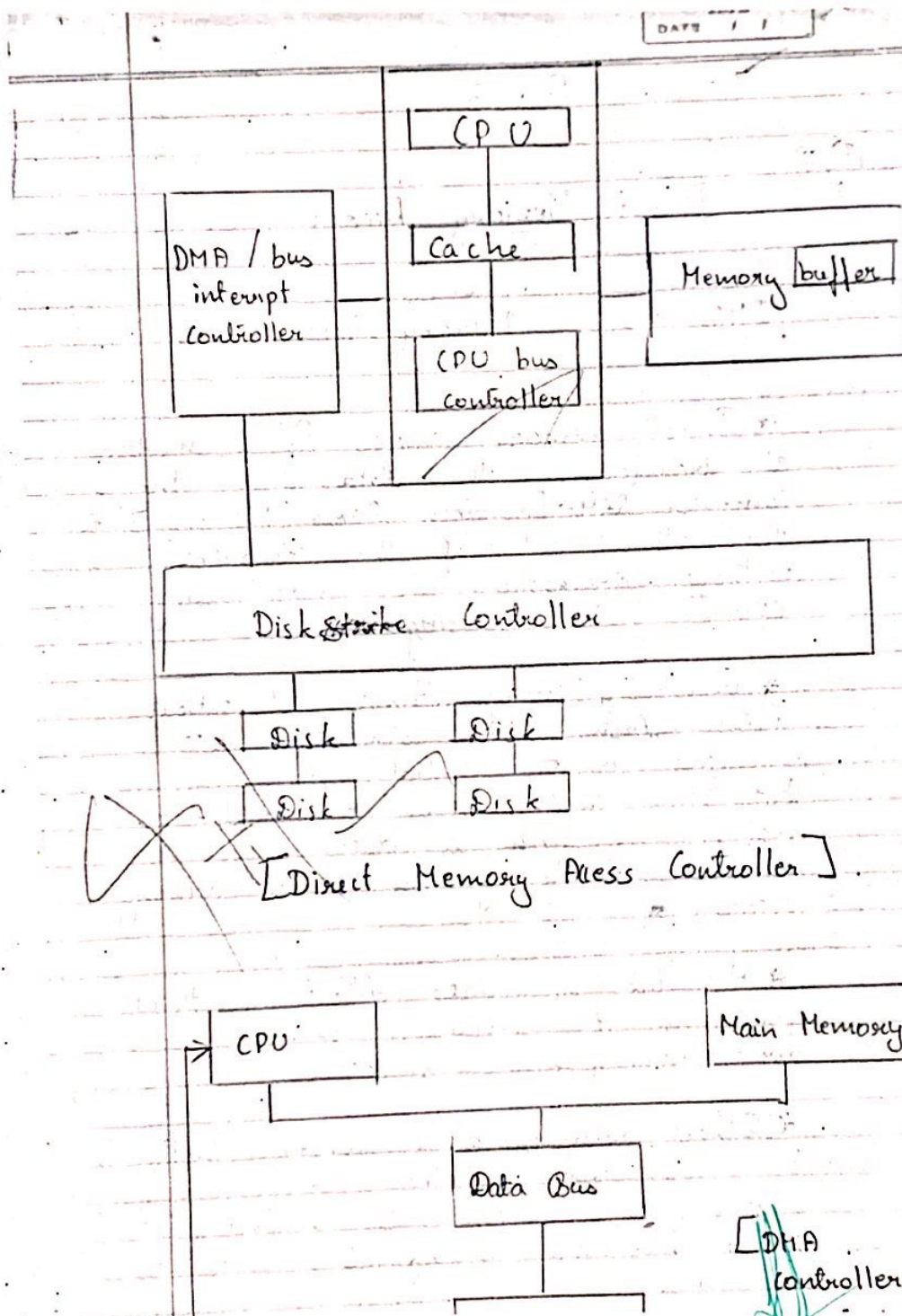
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(1) i)

Storage Devices

Memory Hierarchy

* In the way of memory hierarchy all the storage devices are ordered or arranged in a specific order.

* The ordering of the storage devices is done by the cost and capacity comparison.

* The higher hierarchy has register, which is highest but more efficient.

* From coming down to the hierarchy, the cost is reduced as per bit, and has high capacity.

Memory Hierarchy Advantages:

* Decrease in cost

* Increase in efficient



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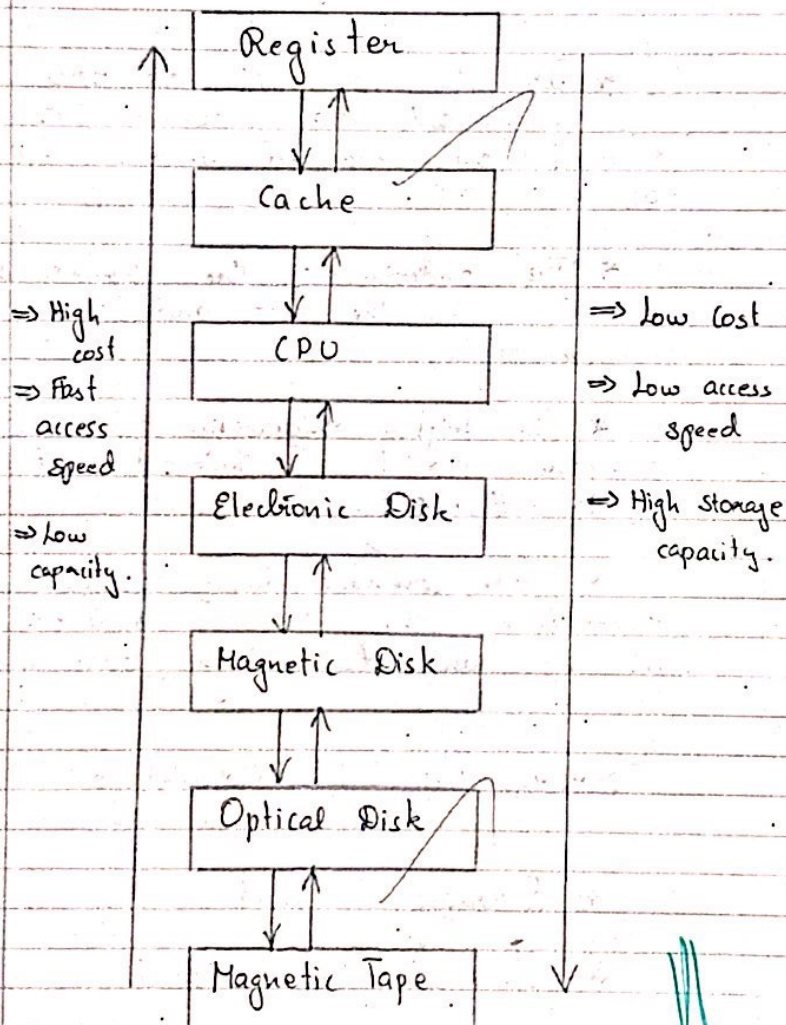
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* Increase in capacity

* Decrease the access times of the memory by the processor.



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* The above figure shows the memory hierarchy of the storage devices.

* The register is a storage device with high cost, fast access time.

* When compare to register cache is less cost, low access time.

* Likewise the cost will be low from top to bottom, but the capacity will increase.

* From bottom to top, the cost will be increase and the access time speed will increasing.

Advantages:

* Decrease in cost

* Increase in efficient

* Increase in capacity

* Decrease the access times of the memory by the processor.



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Q) i) Various Services Provided By Operating System

- 1) Program Development
- 2) Program Execution
- 3) Access to I/O Device
- 4) Access to File
- 5) System access
- 6) Error detection and response
- 7) Accounting
- 8) Instruction System Interrupt
- 9) Application Binary Interface
- 10) Application Program Interface

* These are the various services provided by operating system.



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Program Development: The operating system provide various services to the computer and user, such as editor and debugger assist the user or programmer to develop the program.

Program Execution: There are various steps are involved for the execution of program, such as

- i) Loading the instruction and data in the main memory.
- ii) I/O device and data has to be readed
- iii) And other instruction has to ready

The Operating system controls the scheduling.

Access to I/O Device: Each I/O device must need some resources to process. If the resource is available the operation proceed otherwise the device has to wait until the resource is available.

Access to File I/O Device: Each I/O device has its own peculiar set of instruction or control signal.

Accounting: A good operating system will have a statistics of the process and account the performance.

System Access: System access of public system has a operating system access to system which



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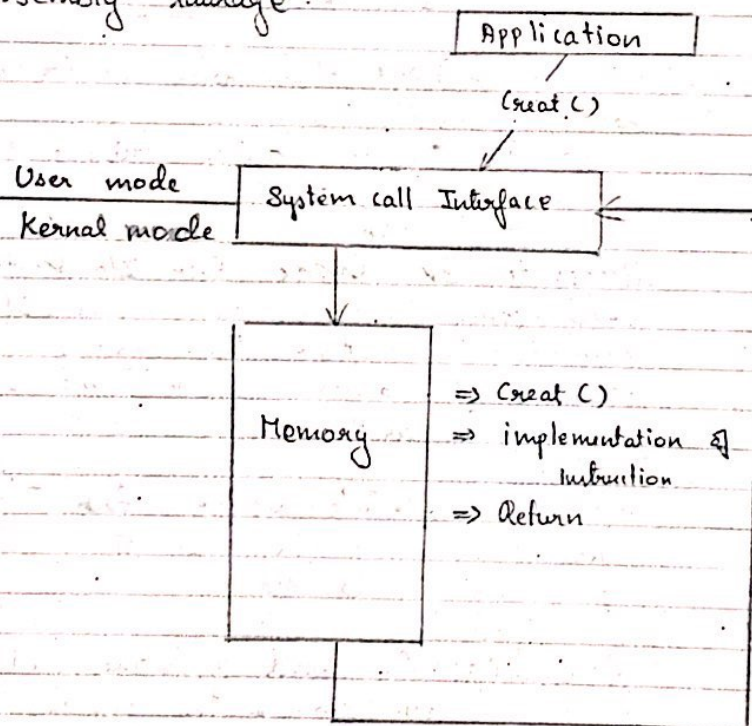
20) ii)

The various types of system calls

System calls:

* System calls provide a interface between the processor and operating system

* The system calls are available in the assembly language.



* There are five major categories types in system call they are



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- * Process Control
- * File Management
- * I/O Device Management
- * Instructions Maintenance
- * Communication

Process Control :

* The running program must to be able to halt at a execution time, normally or abnormally.

* The error is written to the disk and corrected or controlled by the processor.

Example:

=> load execute

File Management :

* Once the program is created, the program has to open and we can read or write or reposition it.

* And finally the program file has to close, which indicates thus we are not using the file longer.

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Example: Create Delete
Open close
Read Write Reposition

I/O Device Management : Each device must need some resources to process. If the resources are available it proceeds and control return to memory otherwise it has to wait for the availability of the resources.

Communication :

* There are two major blocks in interconnected communication, they are:

* Memory shared block

* Message exchange block

Example:

* Sending and receiving message

* Status sharing

Application Maintenance :

* Most system calls exist to interconnect the user and the OS

Eg: * Get process set process

* Get data set data



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Exam Cell

Ref: MAMSE/ACD/2019-20/Even/01	Date: 05.02.2020
Origination: Principal	Classification: Routine
Subject : CIARETEST - I	

The CIARETEST - I examination for II, III & IV B.E students will start from **02.02.2020** and time table is displayed on the notice board. The scheduled time for the test is from **4.30 p.m. to 6.30 p.m.** The portion for the test will be first **TWO UNIT**. All the students are asked to assemble in their respective seats by 4.20 p.m and the students are ^{not to be} not permitted into the exam hall after 4.20 p.m. The students are asked to bring all the required test note, question bank and stationery items.

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Dr. P.RANJITH KUMAR, M.E., P.D.
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All II, III & IV year classes

Notice board

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Retest - Duty list

Date: 05.02.2020

Hall No.	Name of the invigilator	Time	Signature
MB 205	K.Umarani	3.00	K. Umarani
	K.M.Sridhar	3.00	K.M.Sridhar
MB 302	P.Sivamalar	3.20	P.Sivamalar
	R.Premkumar	3.00 PM	R. Premkumar
MB 304	M.Manikandan	3.00 PM	M. Manikandan
	Mr.Saravanan	3.00 PM	Mr. Saravanan
MB 305	S.Ravichandran	3.00	S. Ravichandran
	K.Sathishkumar	3.05	K. Sathish Kumar
MB 307	Mr.Vijayakumar	03.00	Mr. Vijayakumar
	Mrs.Vidhya	3.05	Mrs. Vidhya
MB 308	K.Karthikeyan	03.00	K. Karthikeyan

C. Meena

3.10

5/2/20

Squad Members:

- K.Parthiban / K. Parthiban
- M.Arumugasamy / M. Arumugasamy
- Ms.Dhanalakshmi

G. SATHISH KUMAR - G. Sathish Kumar

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M.A.M. School of Engineering Siruganur, Trichy 621105

CIA – I Retest Hall Plan

Date: 06.02.2020

Hall No.	Year & Dept	No. of Students	Total No. of Students
MB 205	II MECH	26	53
	II AERO	15	
	II ECE	12	
MB 302	III MECH	28 (1 ST)	55
	IV MECH	27 (1 ST)	
MB 304	III MECH	27 (2 ND)	53
	IV MECH	26 (2 ND)	
MB 305	II MCT	16	56
	III MCT	16	
	IV MCT	6	
	IV EEE	18	
MB 307	II CSE	14	56
	III CSE	14	
	IV CSE	11	
	IV AERO	17	
MB 308	III EEE	18	58
	III ECE	8	
	IV ECE	5	
	II EEE	18	
	III AERO	9	

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ATTENDANCE SHEET FOR CIA EXAM-I (Retest)

Hall No. : MB 305

Date : 05.02.2020

S.No	Dept	Reg.No	Name	Signature	No. of additional sheet
1	III AERO	812117101001	ABDUL RAHMAN K	[Signature]	
2	III AERO	812117101002	ABIRAMI M	[Signature]	
3	III AERO	812117101003	AJITH KUMAR V	[Signature]	
4	III AERO	812117101004	ARUNKUMAR M	[Signature]	
5	III AERO	812117101006	CHARULATHA R	[Signature]	
6	III AERO	812117101012	JAYA PRAKASH R	[Signature]	
7	III AERO	812117101015	KATHIRAVAN C	[Signature]	
8	III AERO	812117101026	PRADEEPAN R	[Signature]	
9	III AERO	812117101032	SATHISH S	[Signature]	
10	III AERO	812117101034	SOUNTHIKARAJAN P	[Signature]	
11	III AERO	812117101037	THANISH P	[Signature]	
12	III AERO	812117101040	MOULI M	[Signature]	
13	IV AERO	812116101001	AJELTH K	[Signature]	
14	IV AERO	812116101002	ALEX NUANTHAN M	[Signature]	
15	IV AERO	812116101006	KOWSALYA V	[Signature]	
16	IV AERO	812116101009	MATHESH M	[Signature]	
17	IV AERO	812116101021	SATHISH RAJS	[Signature]	
18	IV AERO	812116101023	SURESH KANNAN K	[Signature]	
19	IV AERO	812116101026	LAMIL SELVAM S	[Signature]	
20	IV EEE	812116105004	ARUN KUMAR A	[Signature]	
21	IV EEE	812116105006	BANISHAGANDHIMATHI P	[Signature]	
22	IV EEE	812116105007	GOWTHAM K	[Signature]	
23	IV EEE	812116105011	M.KALAISELVAN	[Signature]	
24	IV EEE	812116105020	MONIKA P	[Signature]	
25	IV EEE	812116105021	MUGIL SURIYA P	[Signature]	
26	IV EEE	812116105016	A.MAHAVISHNU	[Signature]	
27	IV EEE	812116105022	K.NAVEENKUMAR	[Signature]	
28	IV EEE	812116105023	NAVEEN KUMAR M	[Signature]	
29	IV EEE	812116105025	RAGUL DRAVID K	[Signature]	
30	IV EEE	812116105026	P.RAJARAJAN	[Signature]	
31	IV EEE	812116105027	S.SARAVANAN	[Signature]	
32	IV EEE	812116105028	R.SKRINATH	[Signature]	
33	IV EEE	812116105029	R.YUVASRI	[Signature]	
34	III MCT	812117115002	Ahmed Rifath S	[Signature]	
35	III MCT	812117115006	Harisharadas G	[Signature]	

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M.A.M. School of Engineering Internal Exam Cell CIA - I (Retest) - Absentees List

Dept	Year	Date: 05.02.2020	
		Reg.No. of Absentees	Total No. of Abs
AERO	II	01.05.09,13	4
	III	03.06.12,15,26,37	6
	IV	01,21,25,26	4
CSE	II	02,04,08,19	4
	III	06.17	2
	IV	03,10,14	3
ECE	II	02,06,08	3
	III	28,301	2
	IV	18,20	2
EEE	II	01,03,07,09,10,11,12,13,17	9
	III	NIL	0
	IV	06,20,29	3
MECH	II	06,14,15,16,17,20, 22,23,32,37	10
	III	04,05,06,07,12,14,22,27,28,3 5,36,39,44,54,56,57,58, 59,61,64,67,70,80,81,82,83,8 9,701,702,703	30
	IV	01,03,04,19,31,35,38, 48,59,62,67,501	12
MCT	II	05,08,13,14,23,25,26	7
	III	02,10,19,22,31	5
	IV	NIL	0
Total			106

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9/10/20
6/1/20

Reg no - 312118101223
Name - R. Rajma Devi
Sub - operating system - CS2423
Date - 9/12/2020
Exam - CIA-1 Set 21
Dept - CSE II year

PART-A

1) The Advantage of peer-to-peer systems:

- * The main advantage of peer to peer system over client-server system is that it is easier to set up.
- * The peer to peer system is cost efficient and less expensive.
- * In peer to peer system, all the nodes are server as well as client. Therefore there is no need for additional server.

2) Purpose of system program system call:

System call allow user level process to request services of the operating system.



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3) Interrupt differ from a trap

* Interrupt is a hardware generated signal in which the flow of signal changed within the system.

* While trap is a software generated interrupt. trap is mainly used to catch the trap.

4) Timesharing in multiprogramming

Multiprogramming increases CPU utilization by organizing jobs so that the CPU always has one to execute.

5) Compare and contrast DMA cache memory

* DMA technology provides special channels for CPU and I/O devices to exchange I/O data and the memory is used for buffering the I/O data.

* Caches are automatically managed in that the hardware, when the requested memory contents are not in cache.

6) Traps

Traps is a software generating interrupt. The traps be generated intentionally by a user program, because the traps are mainly used to catch the arithmetic errors.



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10) Dual mode operation and need:

In multiprocessor systems, failure of one processor will not halt the system, but only slow it down. If there are 10 processors and if one fails the remaining processors pick up work from the failed processor.

11) Real Time System:

The system must then be configured or generated for each specific computer size, a process sometimes known as system generation.

12) Clustered System:

Clustered system is one that must react to inputs and respond to them quickly. A clustered system has well defined, fixed time constraints.

13) main purpose of operating system:

- * To provide an environment for a computer user to execute program.

- * To allocate the separate resources of the computer as needed to solve.

- * As a control it serves major functions.



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part - B

16]

i) Pros of multiprocessor systems:

Throughput - Throughput increases because number of processor is increases.

Cost - multiprocessor system is cheaper than the multiple single process system.

Reliability - If one processor fails, it has no effect on whole system operation.

Response time - Response time is less because of increased number of process.

Cons of multiprocessor systems:

* multiprocessor system are more required complex in both hardware and software.

* Additional CPU cycles are required to manage the cooperation. So per CPU efficiency goes down.

* multiprocessor systems are of two types: Symmetric multiprocessing and Asymmetric multiprocessing.

Pros of clustered system:

Resource sharing: + Sharing of software resources such as software libraries, database and hardware.

High reliability - Reliability refers to the degree tolerance against error and component failures.



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Better price performance ratio - Reduction in the price of multiprocessor and increasing computing power gives good performance.

Incremental growth - To excellent power and functionality of a system by simply adding additional resources to the system.

Cons of distributed system:

* There are no current commercially successful examples.

* Protocol overhead can dominate computation costs.

* Hard to build well.

* Probably impossible to build at the scale of internet.

ii) various system call:

* System call provide the interface between a user program and the operating system. Any single CPU computer can execute only one instruction at a time.

* Operating system provides service and system call provides interface to these services. System call is written in language C and C++ as routines.

TNPL



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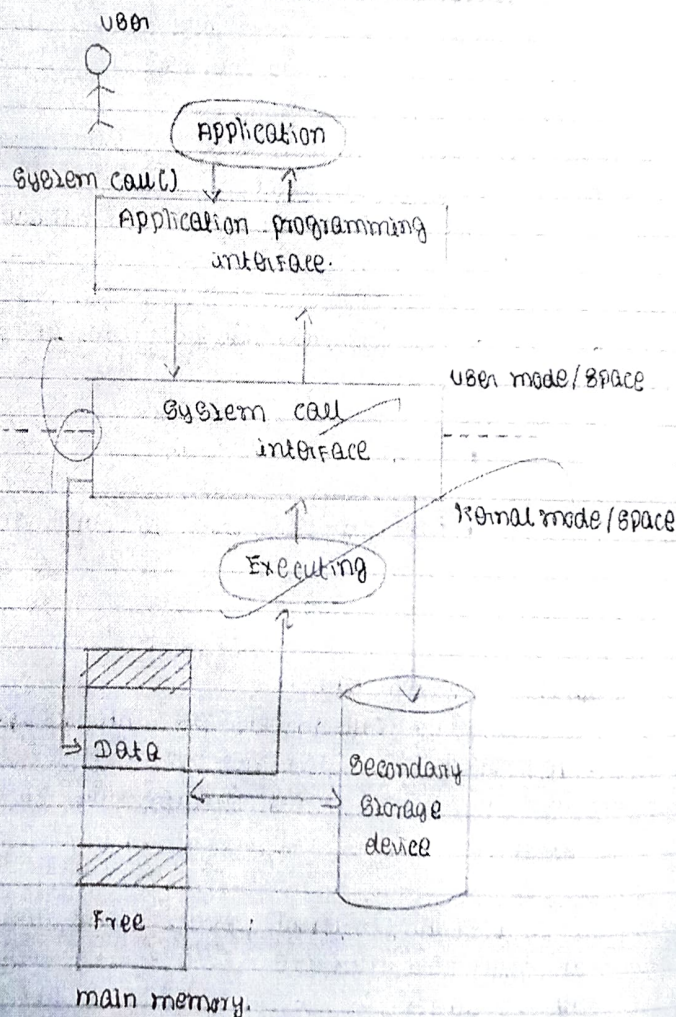
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* System call is technique by which a program executing in user mode can request the kernel service.

* An application programmer interface is a function definition that specifies.





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17)

i) Storage Device

memory hierarchy

* In the way of memory hierarchy all the storage devices are put in an arranged in a specific order.

* The ordering of the storage devices is done in the cost and capacity comparison.

* The higher hierarchy has register which is highest but more efficient.

* From coming down to the hierarchy, the cost is reduced to for but and has high capacity.

Memory Hierarchy Advantage:

* Reduce in cost

* Increase in efficient

* Increase in capacity

* Decreases the capacity lives of the memory by process.



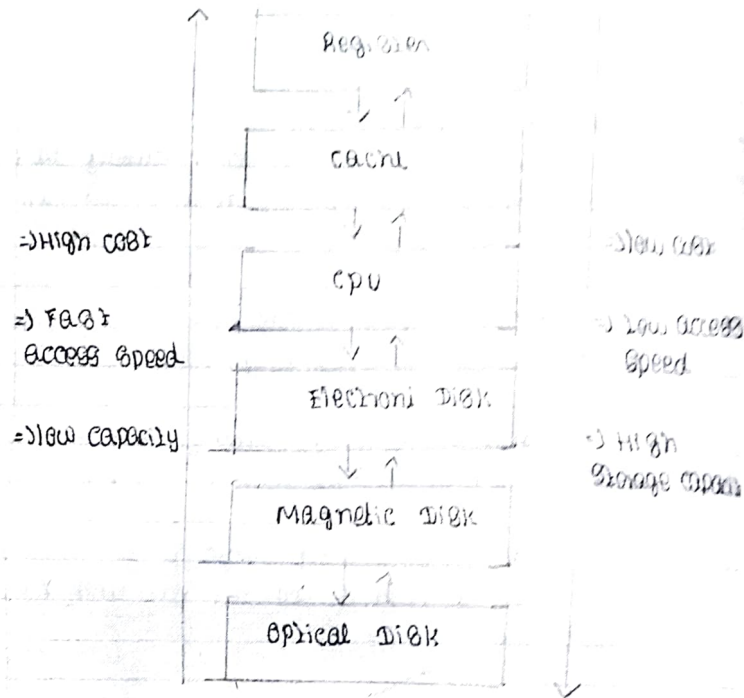
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* The above figure shows the memory hierarchy of the storage devices.

* The register is a storage device with high cost, fast access time.

* When compared to register, cache is less cost, low access time.

* Likewise the cost will be low from top to bottom. The cost increases.



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ii) Direct memory Access

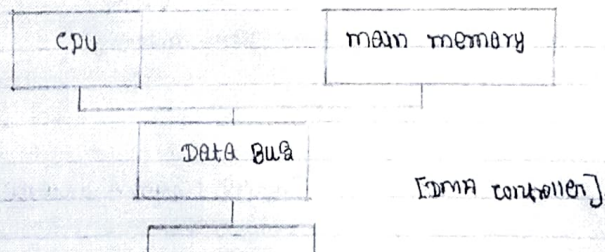
* Direct memory Access is a method of transferring the data from the complex RAM [Random Access Memory] to the other parts of the complex without processing the data using CPU [central processing unit].

* Generally many input and output data from the computer in process by the central processing unit. But data are accessed directly by the direct memory Access.

* Accessing the data directly without the processing in CPU is called direct memory Access process.

* Direct memory Access function can be performed by the direct memory Access module which in the system bus are interconnected with the I/O device.

[Direct memory Access controller]





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19)

i)

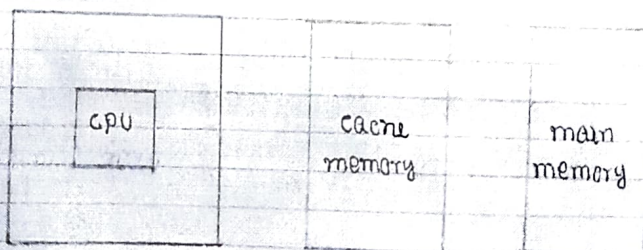
cache memory

* cache is small high speed memory it is derived from SRAM.

* caches are useful. Two or more computers need to exchange data, and the computers perform transfer at different speeds. caches solve the transfer problem by providing a buffer or intermediate speed.

* caches are useful because they can increase the speed of the average memory access and they do so without taking up as much physical space.

* Data is normally kept in storage system. When it is required, it is copied into a faster storage system.



Storage capacity increase →

Access time decreased →



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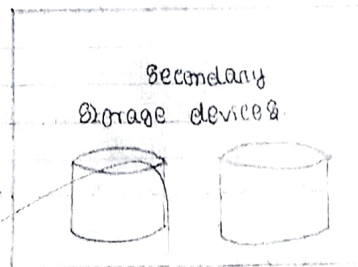
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* If the fast device finds the data it needs in the cache, it need not wait for the slower device.

* making a cache as large as a disk would be ineffective because it would be too costly, the immense size would slow it down and a cache is generally a volatile memory.



ii) Instruction Execution:

The program which is to be executed is a set of instructions which are stored in memory. The central processing unit executes the instructions of the program to complete a task.

The major responsibility of the instruction execution is in which the CPU. The instruction execution takes place in the CPU register.

A special register contains the address of the instruction. The CPU fetches the instruction from memory at address.



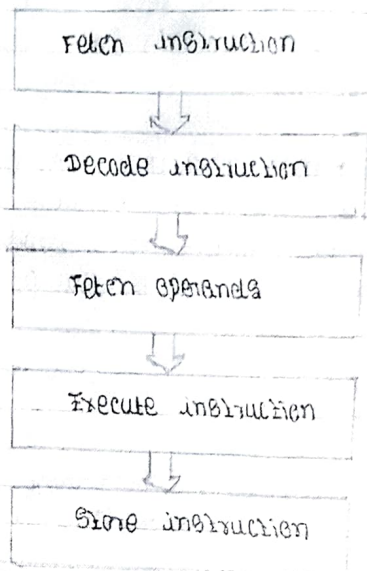
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Instruction Execution Table

The register uses instruction:

Memory Address Register (MAR) - It specifies the address of memory location from which data instruction

Program Counter (PC) - It keeps track of the instruction which is to be executed next, after the execution.

Instruction Register (IR) - Here the instructions are loaded before the execution.



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2a)

i) Various Service provided By

Operating System

1) prepare Development

2) program Execution

3) Access to I/O Device.

4) Access to File.

5) System Access.

6) Error detection and response.

7) Accounting.

8) Instruction System Interrupt.

9) Application Binary Interface.

10) Application Program Interface.

* These are the various Service provided by
Operating System.





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Program Development:

The operating system provide various services to the computer and users, such as editor and debugger assist the user on program to develop the program.

Program Execution:

These are various steps are involved for the execution of program, such as:

- i) loading the instruction and data in the main memory.
- ii) I/O device and data has to be readed.
- iii) And other instruction has to ready.

Access to File:

Each I/O file must need some resource to process. If the resource is available the operation processed otherwise the device has to wait until the resource is available.

Accounting:

A good operating system will have a balance of the process and account the performance.

System Access:

System access of public system has a operating system access to system.



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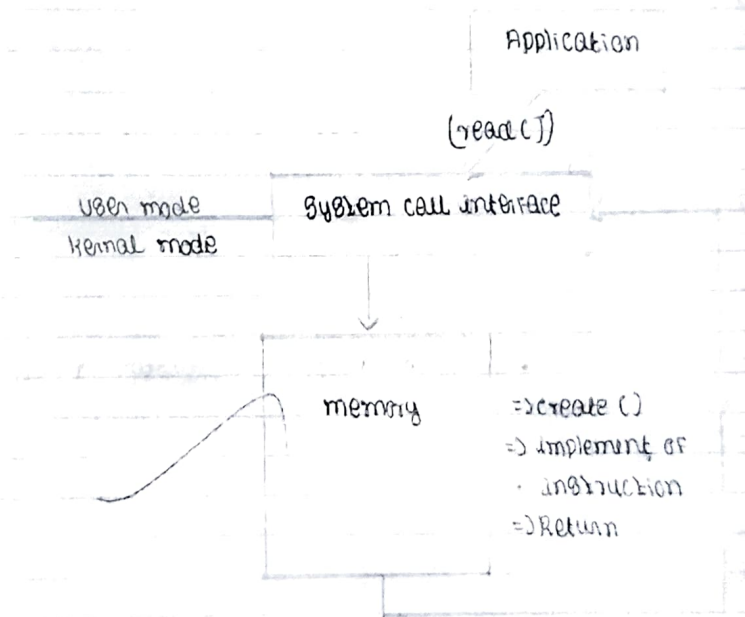
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ii) The various types of system calls

System calls:

- * System calls provide a interface between the processor and operating system.
- * The system calls are available in the assembly language.



* There are five major types in system call they are

- * process control
- * file management
- * I/O device management



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* Instruction maintenance

* Communication

Process control:

* The running program must be able to halt at a execution time, normally or abnormally.

* The error is written to the disk and committed or controlled by the processor.

Ex:

load execute

File management:

* Once the program is loaded, it would be the open and we can read or write or reposition it.

* And finally the program file has to close, which indicates that we are not using the file any more.

Ex:

- * Create Delete
- * open close
- * Read write Reposition



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WEB PORTAL ENTRY

(Period from: 13/1/2020 To: 6/1/2020)

S.No	Reg.Id	Student Name	MAM52		CS4191-CA		CS4492-DBMS		CS4451DAA		CS4493 OS		CS4494-SWEngg	
			Attend ence	Mark	Attend ence	Mark	Attend ence	Mark	Attend ence	Mark	Attend ence	Mark	Attend ence	Mark
1	812118104002	Appuraj R	12	53	12	82	13	55	12	82	12	34	8	45
2	812118104003	Arikaran S	14	100	14	100	13	100	12	100	14	100	8	90
3	812118104004	Aruna M	6	45	6	50	13	91	4	78	11	12	1	45
4	812118104006	Guru Prakash M	14	55	14	55	9	70	11	94	11	49	8	45
5	812118104008	Lopeshwaran S	12	53	12	55	13	55	12	55	11	4	8	45
6	812118104009	Mohamed Aslam K	14	91.9	14	92	13	91	12	100	14	96	12	91.9
7	812118104010	Mohammed Nazem N	13	82.9	13	55	13	55	12	100	13	92	12	82.9
8	812118104011	Mohamed Riyas M	14	100	14	85	9	74	12	100	14	100	12	100
9	812118104012	Muthuselvi A	14	55	14	92	13	83	12	92	14	85	12	55
10	812118104013	Nithya M	12	53	12	89	13	82	13	100	12	89	11	55
11	812118104014	Pandi P	14	93.7	14	93	13	97	12	100	14	92	12	93.7
12	812118104015	Pavithra A	14	100	14	88	13	100	12	100	14	100	12	100
13	812118104016	Preja G	14	92.8	14	100	13	100	12	100	13	95	10	88.8
14	812118104017	Preethika S	13	91	13	91	13	94	12	100	13	97	12	91
15	812118104018	Priyanka K	14	93.9	14	99	13	100	12	100	14	100	12	93.9
16	812118104019	Rajadani P	5	1.8	5	0	8	45	7	48	9	0	9	5.8
17	812118104020	Ranjani C	14	55	14	55	13	55	12	96	14	83	12	55
18	812118104021	Ranjith Kumar R	14	55	14	87	13	88	12	100	14	94	12	55
19	812118104022	Ravivarma S	13	55	13	46	13	55	12	85	13	82	12	55
20	812118104023	Rajana Devi R	14	83.8	14	100	13	82	12	99	14	89.1	11	83.8
21	812118104024	Selvakumar B	8	45	8	45	11	53	12	85	13	60.7	9	40
22	812118104025	Sorvik Prakash K	10	45	10	55	7	0	9	82	13	55	7	45
23	812118104026	Vinitha V	11	94	11	52	13	87	10	93	12	80.9	10	96
24	812118104027	Vineetha R	14	100	14	100	13	95	12	100	14	92	12	100

Staff Signature

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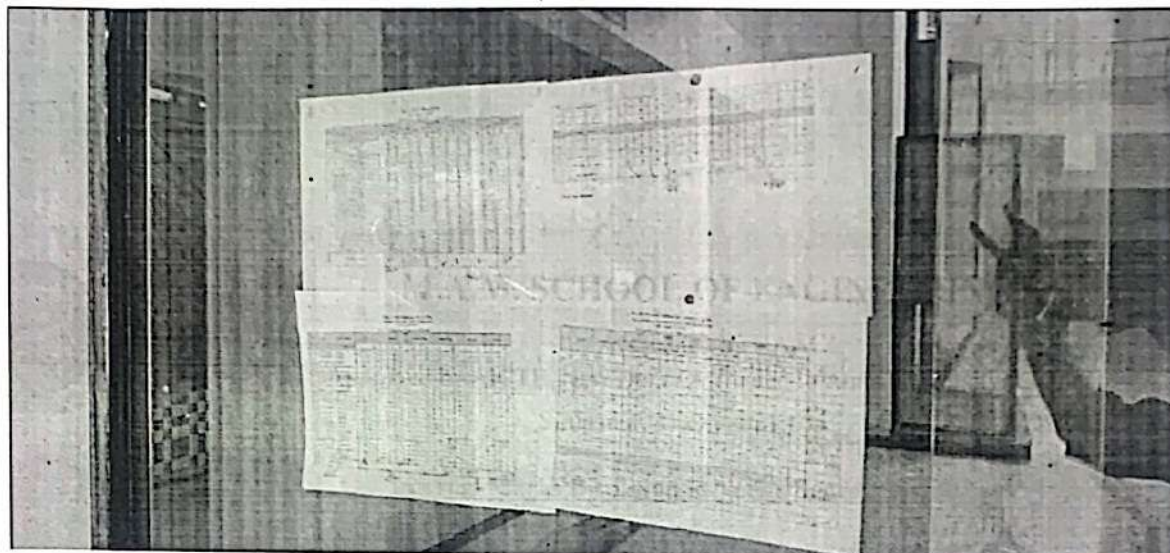
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STUDENT PROGRESS DETAILS

Student Name : K.Mohamed Aslam
Semester : IV Year: II Branch : CSE
Current Semester Attendance Percentage from (13.01.2020 TO 01.2.2020) : 100%

CIA II Test Performance

S. No.	Sub.code	Subject Name	CIA - II Marks Out of 100	Remarks Pass/Fail
1.	MA8452	Probability and Queuing Theory	92	Pass
2.	CS8491	Computer Architecture	91	Pass
3.	CS8492	Database Management Systems	91	Pass
4.	CS8451	Design and Analysis of Algorithm	100	Pass
5.	CS8493	Operating Systems	96	Pass
6.	CS8494	Software Engineering	92	Pass

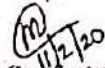
CIA II Test Performance

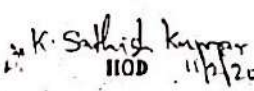
Remarks : Parents have to contact CC through Phone Call after receiving this letter. (பெற்றோர்கள் இந்த கடிதம் கிடைத்த பின்னர் தொலைபேசி அழைப்பு மூலம் வகுப்பு ஆசிரியரை (Ph.No.7530050347) தொடர்பு கொள்ளவும்).

Parents have to meet the HOD on or before. (பெற்றோர் 15.02.2020 HODஐ சந்திக்க வேண்டும்)

NOTE:

தங்கள் மகன்/மகள் வருகை பதிவு 75% குறைவாக இருந்தால் அண்ணா பல்கலைக்கழக தேர்வுக்கு அனுமதிக்க இயலாது, தற்போது 100% வருகை பதிவே உள்ளது. எனவே தாங்கள் துறை தலைவரை 15.02.2020 குள் சந்திக்குமாறு கேட்டு கொள்கிறோம்.


Class Coordinator


HOD


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Department : Mechatronics Engineering
Year / Semester : IV / VII
Sub Code and Name : MT 6011 Project Work
Batch Final List on 1st Review Date : 18.02.2020

Batch Final Unit on I Review Date: 18.02.2020														
Batch No	Reg Number	NAME	Title of Project	Guide Name & Designation	problem formulation	knowledge/understanding of the project	review of the literature	planning and Scheduling of project	implementation	team work	creativity for design work	originality of the project	quality of the project	final grade
I	812116115001	Akhin Kumar.A	Investigation of process parameter in wire EDM, for Inconel 603 XL.	Mrs.Sathya P	5	5	5	5	5	5	5	5	5	5
	812116115002	Arin Kumar H			3	1	2	3	2	2	2	3	1	0.9
II	812116115003	Balavenkatesh.C	Investigation of welding parameter for AISI302 to AISI304 in chemical industry	Mr.Chandrasekar.M	3	3	2	3	4	2	3	3	1	2.2
	812116115004	Gokaraju.S			3	1	1	1	2	2	2	1	1	1.3
III	812116115005	Elugathir.M	Optimization machining parameter for EN18 in serial cranes	Mr.Karthikeyan.S	3	2	1	3	1	2	2	2	2	1.9
	812116115006	Gowda K			3	2	1	3	1	2	1	1	1	1.6
IV	812116115007	Manjula M	Optimization process parameter for honing robot in one turning using desirability function analysis	Mr.Chandrasekar.K	AB									
	812116115008	Magesh Kumar.B			2	0	2	2	1	2	2	1	2	1.5
V	812116115009	Muralidharan.M	Analysis of low wind speed windcraft airfoils	Mr.Aaromagnam.M	OD									
	812116115010	Nikesh.M			2	3	2	3	3	2	2	3	2	3.25
VI	812116115011	Prasanth P	Analysis of pulse on time on hole size and radial over cut on an with EDM	Mr.Saravanan.S	1	1	1	2	2	1	2	3	2	0.15
	812116115012	Ramachandran C.			2	3	2	3	3	2	2	3	2	3.25
VII	812116115013	Sankar B	Investigation of pulse on time on hole size and radial over cut on an with EDM	Mr.Saravanan.S	3	3	3	3	3	3	3	3	2	4
	812116115014	Thamilselvan K			1	2	2	1	2	3	2	3	2	1.1
VIII	812116115015	Vaitheswaran V	Investigation of tensile and wear properties of aluminium metal matrix composite	Mr.Selva prasad	2	2	1	3	3	1	2	2	1	2.1
	812116115016	Vijaya Kumar.K			OD									
IX	812116115017	Vishal Kumar.K	Investigation of tensile and wear properties of aluminium metal matrix composite	Mr.Selva prasad	OD									
	812116115018	Vishal Kumar.K			OD									
RAVICHANDRAN S. AP/MECHT Project Coordinator					P.SUDHA, AP/MECHT HOD/MECHT					Dr.K.Chandrasekar Review Member 1				
										A. Mithambaram Review Member 2				

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First Review

- o Held after about one month from the date of Zeroth review.
- o The PowerPoint Presentation to be made covering the following-
Functional/simulation diagram/hardware Implementation, Completed Coding/
simulation diagram (if any).
- o External Expert member from industry or other institutions may be deputed for this review and further reviews.

Format No 2 : Project Evaluation Form - Review 1						
Project ID		1				
Project Team						
Project Title <u>Investigation of process parameter in wire EDM for Precious</u>						
Sl.no	Register Number	Name of the Students	Guided By			
1.	812116115001	Abhinav Kumar A	Mrs. P. Sudha			
2.	812116115002	Arjun Kumar A				
TEAM MEMBERS CONTRIBUTION AND PERFORMANCE						
Rubrics for Assessing the Progress Work						
1- Not Relevant	2- Marginal	3-Average	4-Good	5-Excellent		
Evaluation Components		Marks	Team Members			
			1	2	3	4
Problem Formulation		5	3	3		
Knowledge/ Understanding of the Project		5	1	1		
Review of the literature		5	2	2		
Objectives and Methodology of proposed Work		5	3	3		
Presentation		5	2	2		
Team Work		5	2	2		
Planning For Future Work		5	2	2		
Originality of the Proposed work		5	3	3		
Is the guide has gone through the PPT?		5	1	1		
Viva Voce		5	0	0		
Total		50	19	19		
Project Assessment Committee		Designation	Comments		Signature	
1	HOD	Need more references				
2	Project Coordinator	More Collaboration				

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Department of Mechatronics Engineering

IV Year Mechatronics

1st Project Review Attendance Sheet Date : 18.02.2020 PN-AN

S.NO	Batch No	Reg Number	NAME	Signature	Remarks
1	I	812116115001	Abinas Kumar.A		19
2		812116115002	Arun Kumar R		19
3	II	812116115003	Balamurugan.G		26
		812116115006	Gunaseelan.S		15
4	III	812116115004	Elangathir M		19
		812116115005	Gowsalya K		16
7	IV	812116115007	Manisha M	AB	AB
8		812116115008	Mugesh Kumar.B		15
9		812116115009	Muralidharan.M	OD	AB
10	V	812116115010	Nitheesh.M		25
11		812116115011	Prasanth P	present	15
12		812116115012	Ramachandran C		25
13	VI	812116115014	Sankar B		30
14		812116115015	Thamilselvan K		19
15	VII	812116115016	Vaitheswari V		19
16		812116115017	Vijaya Kumar.K	OD	AB
17		812116115018	Vinith Kumar.K	OD	AB

P.SUDHA, AP/MECHT
HOD/MECHT

18/2/20
Co-ordinator
1. P. S. Chandrasekhar
2. M. J. [Signature]
Review Members

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Department of Mechatronics Engineering
IV Year Mechatronics

II nd Project Review Attendance Sheet Date : 16.3.2020 EN / AN

S NO	Batch No	Reg Number	NAME	Signature	Remarks
1	I	812116115001	Abinas Kumar.A	<i>[Signature]</i>	37
2		812116115002	Arun Kumar R	<i>[Signature]</i>	37
3	II	812116115003	Balamurugan.G	<i>[Signature]</i>	39
4		812116115006	Gunaseelan.S	AB AB	AB
5	III	812116115004	Elangathir M	<i>[Signature]</i>	32
6		812116115005	Gowsalya K	<i>[Signature]</i>	32
7	IV	812116115007	Manisha M	<i>[Signature]</i>	36
8		812116115008	Mugesh Kumar.B	<i>[Signature]</i>	36
9		812116115009	Muralidharan.M	AB	AB
10	V	812116115010	Nitheesh.M	<i>[Signature]</i>	35
11		812116115011	Prasanth P	<i>[Signature]</i>	37
12		812116115012	Ramachandran C	<i>[Signature]</i>	36
13	VI	812116115014	Sankar B	<i>[Signature]</i>	36
14		812116115015	Thamilselvan K	<i>[Signature]</i>	35
15	VII	812116115016	Vaitheswari V	<i>[Signature]</i>	34
16		812116115017	Vijaya Kumar.K	AB (OD)	AB(OD)
17		812116115018	Vinith Kumar.K	AB	AB

P.SUDHA, AM/MECHT
HOD / MECHT

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Department : Mechanical Engineering
Year / Semester : IV / VII
Sub Code and Name : ME6501 - Project Work
Batch Final List - B in Realtime Date : 16.3.2020 AN

S.N.	Batch No.	Reg Number	NAME	Title of Project	Guide Name & Designation	5 Marks Each Question & Total of 50 Marks										Total
						problem identification	literature surveying at the project	choice of the material	theoretical and experimental work	size of experiment	time required	cost of material	quality of work	presentation and documentation	is the project report submitted on time	
1	I	81210119001	Ahlan Kumar A	Investigation of process parameter in shot EDM, for Internal G8 K3.	Mrs.Sathya P	4	3	4	2	2	4	4	3	4	5	37
2		81210119002	Arun Kumar B			4	3	4	3	3	4	4	3	4	4	39
3	II	81210119003	Balamurugan C	Evaluation of welding parameter for AISI304 to AISI304 dissimilar metals weld in chemical industry	Mr.Chandrasekhar M	3	3	4	4	4	4	4	3	4	4	32
4		81210119004	Chandrasekhar S			3	3	4	4	4	4	4	3	4	4	32
5	III	81210119005	Elangothir M	optimization working parameter for EN18 in metal crane	Mr.Ramesh Kumar S	3	3	3	3	4	2	3	3	3	4	34
6		81210119006	Elangothir S			3	3	3	3	4	2	3	3	4	4	34
7	IV	81210119007	Manikha M	process parameter analysis for Banana rubber in cast turning using desirability function analysis	Mr.Chandrasekhar M	3	3	4	4	3	4	4	4	4	4	35
8		81210119008	Manikha Kumar B			3	3	4	4	3	4	4	4	4	4	35
9		81210119009	Manikha Kumar M			3	3	3	3	3	4	4	3	4	5	37
10		81210119010	Manikha M			4	3	4	3	4	4	4	3	4	4	36
11	V	81210119011	Pranesh P	Analysis of low wind speed windmill airfoil	Mr.Aaravamanyan M	3	3	4	4	3	4	4	3	4	4	36
12		81210119012	Ramesh Kumar C			4	3	3	4	4	4	4	3	4	3	35
13	VI	81210119013	Sathya B	Experiments of pulse on time on hole size and radial over cut using with EDM	Mr.Chandrasekhar M	4	3	3	4	3	4	4	3	3	3	34
14		81210119014	Thandapani K			4	4	4	3	4	3	3	3	3	3	34
15		81210119015	Vallabhanathan V	Triological study of dissimilar metal matrix composite	Mr.Sathya Sathya	4	4	4	3	4	3	3	3	3	3	34
16	VII	81210119016	Vijaya Kumar K			4	4	4	3	4	3	3	3	3	3	34
17		81210119017	Vijaya Kumar K			4	4	4	3	4	3	3	3	3	3	34

Project Coordinator: RAMESH KUMAR B, AP/MECHT
HOD / MECHT: P. SATHYA SATHYA
Revision Member 1: SATHYA SATHYA
Revision Member 2: SATHYA SATHYA



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Department ofMELHATRONICS ENGINEERING.....

BONAFIDE CERTIFICATE

This is to certify this Practical work titled

.....MT 33.31- ROBOTICS LABORATORY.....

is the bonafide work ofN. MOHAMMED AMEEL.....

Registration Number120705013.....

[Signature]
Staff in Charge

[Signature]
Head of the Department

Submitted for the Anna University Chennai Practical Examination held on 27-03-2021

at M.A.M. School of Engineering, Trichy - 621 105.

[Signature]
Internal Examiner

[Signature]
External Examiner

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2	19/12/20	Verification of transformation	25	9	J. J. J.
3	21/12/20	Estimation of Accuracy, Repeatability and Resolution	51	9	J. J. J.
4	28/12/20	Robot programming and simulation for pick and place	73	9	J. J. J.
5	04/01/21	Robot programming and simulation for colour discrimination	77	9	J. J. J.



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8	3/02/21	Robot programming and simulation for welding practice	80	9	
9	26/02/21	Robot programming and simulation for any Industrial process	93	9	
10	01/03/21	Robot programming and simulation for multi process	97	9	
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